REMARKS

This application has been carefully reviewed in light of the Final Office Action dated July 27, 2007. Claims 1-18 remain in this application. Claims 1-2 are the independent Claims. Claims 1-2, and 5-8, have been amended. It is believed that no new matter is involved in the amendments or arguments presented herein. Reconsideration and entrance of the amendment in the application are respectfully requested.

Art-Based Rejections

Claims 1-18 were rejected under 35 U.S.C. § 102(b) over U.S. Patent 6,157,988 (Dowling).

Applicant respectfully traverses the rejections and submits that the claims herein are patentable in light of the clarifying amendments above and the arguments below.

The Dowling Reference

Dowling is directed to providing a pipeline architecture with a branch caching structure that reduces or eliminates pipeline stalls regardless of whether the fall-through or the target instruction is to be executed. The present architecture is hardware efficient and involves simple parallel operations that can be performed in a short clock cycle. (*See, Dowling, col. 4, lines 15-19*)

The Claims are Patentable Over the Cited References

The present application is generally directed to a data processing device using pipeline control.

As defined by amended independent Claim 1, a data processing device using pipeline control includes an instruction queue in which a plurality of instruction codes are fetched. A fetch address operation circuit calculates a fetch address used to fetch an instruction code in the instruction queue. A fetch circuit fetches an instruction code that is read out based on the fetch address into the instruction queue. A branch information setting circuit decodes a branch setting instruction. The branch setting instruction explicitly or implicitly specifies a branch occurring address and a branch target address. A branch to the branch target address occurs when the fetch address is the branch occurring address after a x-th instruction from the branch setting instruction, the branch information setting circuit stores the branch occurring address in a branch occurring address storage register and the branch target address in a branch target address storage register, when the branch setting instruction is decoded. The fetch address operation circuit includes a circuit which compares one of a previous fetch address and an expected next fetch address with a value stored in the branch occurring address storage register, and then determines whether or not to output a value stored in the branch target address storage register as a next fetch address, based on the comparison result.

The applied references fail to disclose or suggest the above features of the claims of the present invention. In particular, the applied references fail to disclose or suggest "wherein a branch to the branch target address occurs when the fetch address is the branch address...," as required by the claims of the present invention.

Moreover, the applied references fail to disclose or suggest "the branch information setting circuit stores the branch occurring address in a branch occurring address storage register," required by the claims of the present invention.

Amended independent Claim 1 requires that a branch to the branch target address occurs, when the fetch address is the branch address. The Specification of

the instant Application supports this. According to the Specification, Figs. 3C, 5C and 7C P1 and P2 are a branch target and a branch target address, respectively *(see page 15, lines 9 to 13; page 17, line 24 to page 18, line 2 and page 19, line 27 to page 20, line 5).* A person skilled in the art would clearly recognize that a branch address of the present Application does not signify a branch target address

Dowling teaches "branch address (PC+DISP+OFFSET) 706." (*See, Dowling, col. 15, ll. 34 and 35.*) Dowling also discloses "a target fetch address 706," (*id., col. 15, ll. 43, 44, 45.*) According to Dowling, "the branch target address is supplied from the branch cache 702 to the program address generate stage 202 via the line 706," (*Dowling, col. 17, ll. 35 to 37,*) and "The state 912 also assert a multiplexer 718 to provide the output of the shadow dispatch unit 712 to the decode stage 212," (*id. Col. 17, ll. 62 to 64.*)

Thus, Dowling assigns numeral 706 to both a branch address and a branch target address. In other words, the phrases "branch address" and "branch target address," are accorded the same meaning by Dowling. In contrast, the present invention as defined by amended independent Claim 1 requires that "wherein a branch to the branch target address occurs when the fetch address is the branch address."

The Office Action states, "A branch condition must also signify a branch address and a branch target address or else a branch condition is useless." (*See, Office Action, page 4, lines 7 to 9.*) Applicants respectfully traverse this statement.

According to Dowling:

> if the branch condition,...evaluates to fall through, then control is passed from the state 612 over a transition 630 back to the idle state 602. In this case, the fall through addresses will be executed similarly to a delayed branch. (*Dowling, col. 13, ll. 29-32.*)

Dowling further states:

> "the information in a condition field 808 (see subsequent discussion of FIG. 8) may optionally be set to indicate the condition source of the branch instruction and to indicate whether the condition is early-resolvable or not" (*Dowling, col. 13, ll. 14 to 18.*)

Moreover, Dowling discloses that,

> An optional condition field (COND) 808 holds the register or pipeline address of the data that will be needed to resolve the conditional branch. The condition field 808 also indicates if the branch is early-resolvable" (*Dowling, col. 16, ll. 43 to 46.*)

Accordingly, one of ordinary skill in the art would readily recognize that a branch condition of Dowling is not data which determines the branch occurring timing, but data which determines whether it is possible to allow a branch to occur, such as, for example, the result of an instruction which has been executed before a branch instruction.

Clearly, Dowling does not teach that a branch condition means data which determines the branch occurring timing. Accordingly, it is not the case that a branch condition is useless unless a branch condition signifies a branch address. In fact, Fig. 8 of Dowling illustrates TARGET ADD (802) separately from COND (808) at the branch cache (702). Therefore, a branch condition is not a branch target address.

Therefore, Dowling teaches a branch address which has substantially the same meaning as a branch target address. This means a branch occurring address of the present application is different from a branch address of Dowling.

In contrast, the present invention, as defined by amended independent Claim 1, requires "the branch setting instruction explicitly or implicitly specifies a branch occurring address and a branch target address, wherein a branch to the branch target address occurs when the fetch address is the branch occurring address after x-th instruction from the branch setting instruction," recited by amended independent Claim 1. In fact, Dowling is silent about "the branch setting instruction explicitly or implicitly specifies a branch occurring address and a branch target address".

Moreover, as described in paragraph 2.3, Dowling fails to teach the feature "the branch information setting circuit stores the branch occurring address in a branch occurring address storage register," as recited by amended independent Claim 1.

Since the cited reference fails to disclose, teach or suggest the above features recited in amended independent Claim 1, that reference cannot be said to anticipate nor render obvious the invention which is the subject matter of that claim.

Accordingly, amended independent Claim 1 is believed to be in condition for allowance and such allowance is respectfully requested.

Applicant respectfully submits that amended independent Claim 2 is allowable for at least some of the same reasons as those discussed in connection with amended independent Claim 1 and such allowance is respectfully requested.

The remaining claims depend either directly or indirectly from amended independent Claims 1 and 2 and recite additional features of the invention which are neither disclosed nor fairly suggested by the applied references and are therefore also believed to be in condition for allowance.

Conclusion

Applicant believes the foregoing amendments comply with requirements of form and thus may be admitted under 37 C.F.R. § 1.116(b). Alternatively, if these amendments are deemed to touch the merits, admission is requested under 37 C.F.R. § 1.116(c). In this connection, these amendments were not earlier presented because they are in response to the matters pointed out for the first time in the Final Office Action.

Lastly, admission is requested under 37 C.F.R. § 1.116(b) as presenting rejected claims in better form for consideration on appeal.

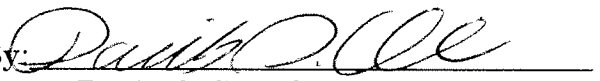
In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (310) 785-4721 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

Date: October 29, 2007

By: 

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